II. AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method of preventing exposure of at least one layer of a semiconductor device, the method comprising the steps of:

etching ~~an opening~~ through an interlevel dielectric (ILD) layer and partially into an underlying cap layer thereby leaving an opening through the ILD layer and a remaining portion of ~~an~~ the underlying cap layer;

maintaining the semiconductor device in an inert gas; and

forming a portion of a liner in the opening to prevent exposure of the ILD layer during subsequent processing.

2. (Original) The method of claim 1, wherein the remaining portion is no less than approximately 10% of the underlying cap layer thickness and no greater than approximately 90% of the underlying cap layer thickness.

3. (Original) The method of claim 1, wherein the portion of the liner is no less than approximately 5% of a total liner thickness and no greater than approximately 30% of the total liner thickness.

4. (Original) The method of claim 3, wherein the portion of the liner is no less than approximately 10% of the total liner thickness and no greater than approximately 20% of the total liner thickness.

5. (Original) The method of claim 1, wherein the subsequent processing includes:

etching through the portion of the liner and the portion of the underlying cap layer to expose a metal layer; and

forming a via in the opening.

6. (Original) The method of claim 1, further comprising the step of degassing prior to the liner forming step.

7. (Original) The method of claim 1, wherein the inert gas is selected from the group consisting of:

argon and nitrogen.

8. (Currently Amended) A method of forming a via in a semiconductor device, the method comprising the steps of:

first etching an opening through an interlevel dielectric (ILD) layer and partially into an underlying cap layer thereby leaving a remaining portion of ~~an~~ the underlying cap layer;

maintaining the semiconductor device in an inert gas;

forming a liner at the ILD layer opening and at the remaining portion wherein at least a portion of ~~a~~ the liner in the opening is configured to prevent exposure of the ILD layer;

second etching through the at least a portion of the liner and the remaining portion of the underlying cap layer to expose a metal layer; and

forming the via in the opening.

9. (Original) The method of claim 8, further comprising the step of degassing prior to the liner forming step.

10. (Original) The method of claim 8, wherein the second etching step is conducted in an etching chamber.

11. (Original) The method of claim 8, wherein the second etching is conducted in a liner deposition chamber.

12. (Original) The method of claim 8, wherein the remaining portion is no less than approximately 10% of the underlying cap layer thickness and no greater than approximately 90% of the underlying cap layer thickness.

13. (Original) The method of claim 8, wherein the portion of the liner is no less than approximately 5% of a total liner thickness and no greater than approximately 30% of the total liner thickness.

14. (Original) The method of claim 14, wherein the portion of the liner is no less than approximately 10% of the total liner thickness and no greater than approximately 20% of the total liner thickness.

15. (Original) The method of claim 8, wherein the portion of the liner includes tantalum nitride.

16. (Original) A method of forming a via in a semiconductor device, the method comprising the steps of:

first etching an opening through an organic interlevel dielectric (ILD) layer and leaving a remaining portion of an underlying cap layer to maintain a metal layer thereunder sealed;

maintaining the semiconductor device in an inert gas;

degassing the semiconductor device;

forming at least a portion of a liner in the opening to prevent exposure of the ILD layer in a chamber;

second etching through the portion of the liner and the portion of the underlying cap layer to expose the metal layer in the chamber; and

forming the via in the opening.

17. (Original) The method of claim 16, wherein the remaining portion is no less than approximately 10% of the underlying cap layer thickness and no greater than approximately 90% of the underlying cap layer thickness.

18. (Original) The method of claim 16, wherein the portion of the liner is no less than approximately 5% of a total liner thickness and no greater than approximately 30% of the total liner thickness.

19. (Original) The method of claim 18, wherein the portion of the liner is no less than approximately 10% of the total liner thickness and no greater than approximately 20% of the total liner thickness.

20. (Original) The method of claim 16, wherein the portion of the liner includes tantalum nitride.